Impact of Chip and Interposer PDN to Eye Diagram in High Speed Channels

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***Abstract*— The paper applies the combined SI-PI co-simulation to on chip high speed interconnects. A complete model of chip and interposer PDN is developed and, together to a lumped model of the PCB and package PDN, it is employed to supply I/O drivers for HBM traces laid out on silicon interposer. A comprehensive analysis is carried out highlighting the impact of the decoupling capacitor placement and their corresponding parasitic inductance on the supply voltage ripple and on the output eye diagram at the signal receivers.**

Keywords—power distribution network, decoupling capacitors, Si-PI co-simulation, eye diagram, high bandwidth memory.

I. Introduction

The trend of modern electronic design in terms of reduction of power consumption, reduction of supply voltage level, and increase of digital data rate calls for a combined SI-PI co-simulation [1]. Each portion of the PDN should be carefully modeled [2], [3] and designed to minimize its input impedance seen by the I/O drivers. Then the PDN should be combined with the channel model to achieve an accurate prediction of the output eye diagram, by taking into account the impact of the PDN such as the power supply induced jitter and the ripple induced on the supply rails [4]. This paper review the complete modeling process of the SI-PI co-simulation highlighting some aspects that should be taken into account during the design of the high frequency portion of the PDN at chip and interposer level. In particular, the novel contribution consists on the identification of the best case eye diagram as a consequence of the decap placed directly at the I/O port; although this is unfeasible due to inherent parasitic inductance, this case represents the target to which the designer should tend while appropriately selecting and placing the decaps. Thus this study provides a strategy to avoid an overdesign of the PDN by an excess of decaps or expensive low inductance decaps.

II. Overview of the PDN Model

A. Construction of the Interposer and Chip PDNs

The geometry of the PDN of interest (chip and interposer PDNs) consists of interleaved power and ground traces laid out on two metal layers and realizing a grid type of structure, as fully described in [2],[3]. The interposer PDN is made by two PWR/GND structures, toward the top and the bottom surfaces, and they are connected by an array of through silicon vias (TSVs). The interposer PDN is then connected to the chip PDN by means of bumps. The details of the overall PDN assembly and of the equivalent circuit derivation are described in [5]. Once the equivalent circuit of the grid structure made by the assembly of a matrix of Unit Cells is obtained, the decoupling capacitors (decaps) at chip and interposer level may be accordingly added. The study carried out in this paper focuses on the impact of the decap placement and value and the modeling problems when a PI/SI co-simulation needs to be performed. To this aim the chip PDN includes the ports to power up the I/O drivers; it includes also additional ports uniformly distributed through the chip area for the connection of the decaps.

B. Placement of Decoupling Capacitors

The case example considered in this paper is based on the configuration in Fig. 1 where the large rectangle represents the interposer footprint, whereas the smaller one filled by a grid of squares is the footprint of the IC (Chip2 in Fig. 1a) placed above the interposer. The dark square are the location where I/O ports and decoupling capacitors (decaps) can be placed [5]. The specific case of interest consists of 4 decaps surrounding Port 1, 2 decaps at Port 2, and no decaps at Port 3. The value of the decap capacitance is set to 1 nF with parasitic resistance equal to 10 mΩ. The decap inductance is varied from 0 pH to 50 pH. An additional case variation is considered where each decap is placed directly at the port, not on the grid, to study the impact of the intrinsic inductance of the UCs between the port and the

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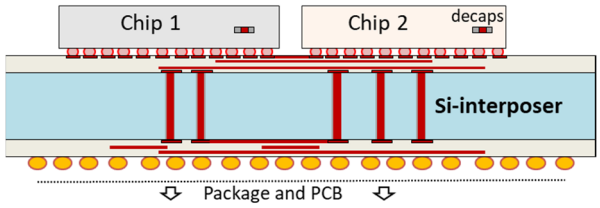
decap. The on-port decap will not be affected by the PDN intrinsic inductance since the decap to port distance is zero.



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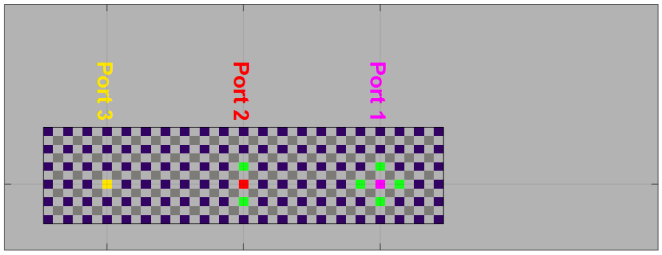


(b)

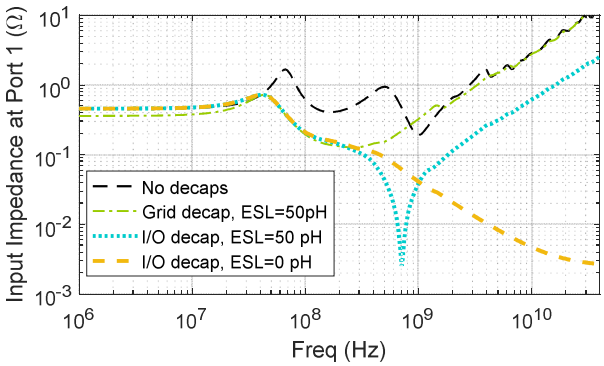
Fig. 1. (a) Overview of the interposer and chip stack-up. (b) PDN footprint of Chip2 (colored squares) on top of the Interposer footprint.

C. *Results of Input Impedance*

The main results of the PDN input impedance are summarized in Fig. 2; in particular the impedance at Port 1, 2, and 3 are shown for all cases. The comparison in Fig. 2 highlights the impact of the inductance as well as of the position of the decaps with respect to the I/O port; the complete lack of inductance makes the curve decreasing beyond 1 GHz; the difference between the decap with 50 pH ESL located at the I/O port and at the grid makes clear the impact of the intrinsic UC inductance. This latter inductance should be carefully considered when the actual position of the on-chip decap is transformed into a discretized coordinate associated to the UC-based equivalent circuit model.

Fig. 3 includes all three impedances for the cases with decaps. The comparisons between the three figures of Fig. 3 highlights the impact of the port to decap loop inductance. Specifically this inductance is larger when the decaps are placed on the grid locations; when the decaps are placed directly at the port, instead, the UC intrinsic inductance should be neglected, and the ESL becomes relevant. The case limit of ESL = 0 makes Z_{11} and Z_{22} very small beyond 1 GHz. Although this ESL value is practically unfeasible, it may represent a useful limit to highlight the inductance impact on the voltage ripple as well as on the output signal eye diagram as will be shown later.

It is worth to note that the overall PDN input impedance in Figs. 2 and 3 is a combination of the chip and interposer PDNs with the lumped element model of the PCB and package PDN shown in Fig. 4 [4].



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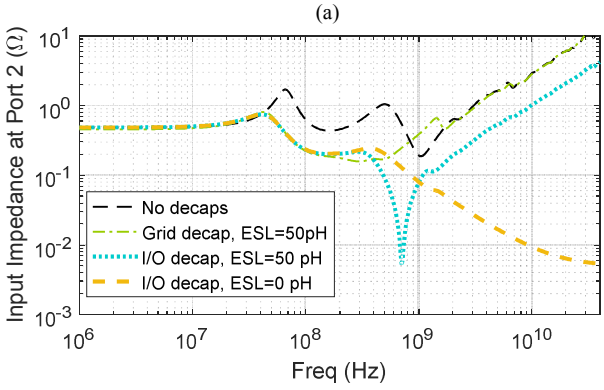

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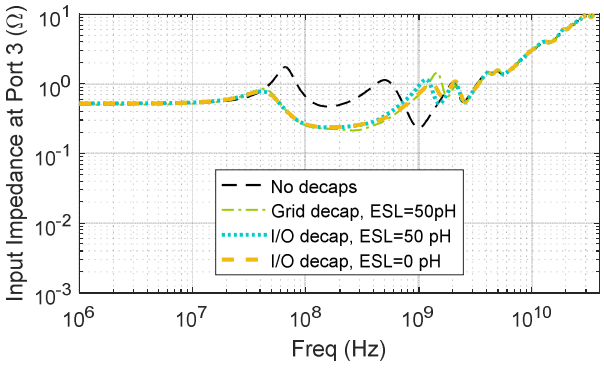
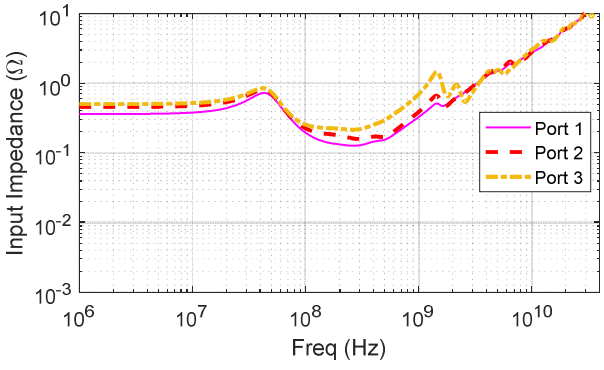


(c)

Fig. 2. PDN input impedance for all cases. (a) Z_{11}. (b) Z_{22}. (c) Z_{33}.



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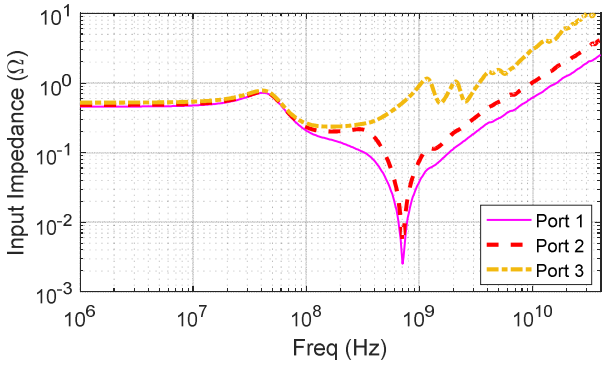

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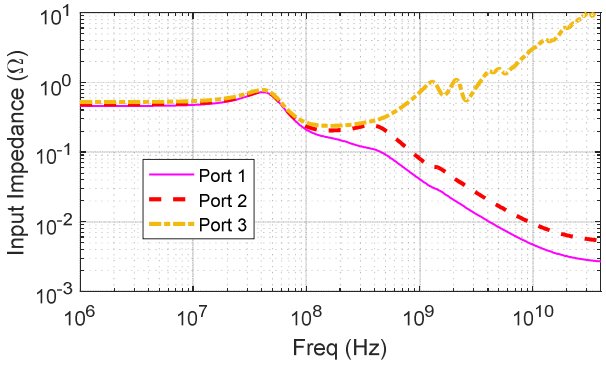


(c)

Fig. 3. PDN input impedance. (a) Case with decaps at the grid (ESL = 50 pH). (b) Case with decaps at the I/O (ESL = 50 pH). (c) Case with decaps at the I/O (ESL = 0 pH).

III. SI/PI CO-SIMULATION FOR HBM CHANNELS

A. *HBM channel co-simulation setup*

The voltage ripple generated on the voltage supply rail due to the non-ideal PDN can propagate to the I/O, thus degrading the output eye diagram. SI-PI co-simulation is used to characterize the PDN influence on the output waveform of the I/O. A HBM channel [4], [6] consists of HBM signal trace, an I/O driver, and the I/O PDN. A microstrip above the silicon interposer in Fig. 1a is used to represent the signal traces going from Chip 1 to Chip 2. Only 3 traces are used for simplicity [4]. The three PDN I/O ports in Fig. 1 are used to connect the driver of the three signal traces. The overall system setup is shown in Fig. 4, where a chain of 7 inverters is used to drive the signal through the large capacitive interposer trace and load. The parasitic and load capacitances are reported in the figure.

B. *HBM channel co-simulation results*

In the system setup shown in Fig. 4, to observe the PDN impacts on the output of the HBM channel, the PDN configurations described in Section II are used. Three PRBS signals with 5Gbps and 50 ps rise/fall time are applied, which will draw current from the I/O drives. This current, due to the non-ideal PDN input impedance, leads to a voltage ripple on the chip power net. An example of the voltage ripple for the case of PDN without decaps added is shown in Fig. 5.

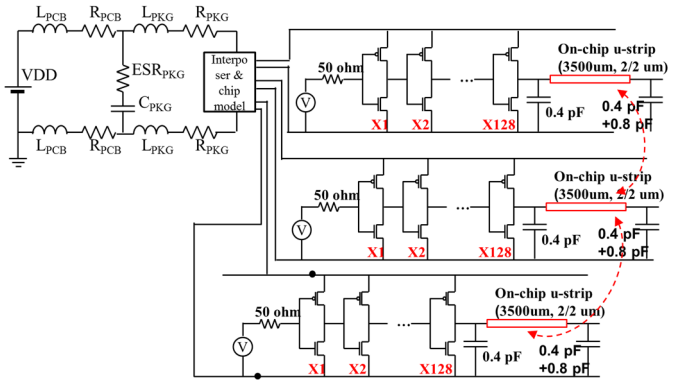
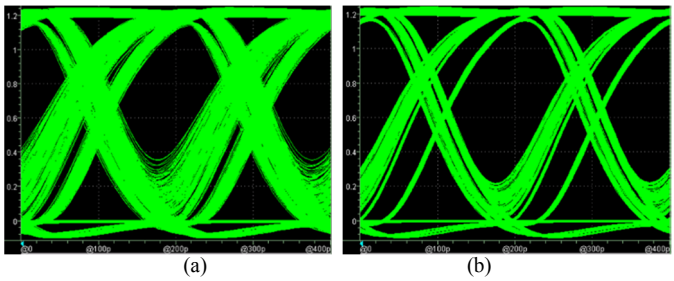


Fig. 4. HBM channel blocks for SI/PI co-simulation

Fig. 5. Voltage ripple at the power net of the I/O Port 1 for the case without decaps.

The voltage ripple on the power net of the I/O can influence the output of the signals traces, and thus it further introduces the so called power supply induced jitter (PSIJ). Also, the noise on the power net can be coupled to the nearby signal traces through crosstalk. In this paper, HPSICE transient simulation is used to obtain the eye-diagram at the trace outputs. Fig. 6a shows the eye-diagram of the Port 3 for the no-decap case. The voltage ripple generated on the power net of Port 3 is 127mV. Fig. 6b and Fig. 6c show the eye-diagram at the output of the Port 3 when decaps having ESL = 0 pH and 50 pH, respectively, are added directly at the port, according to the placement in Fig. 1. By comparing the eye diagrams it is clear that the decaps, being far from Port 3, do not help much reducing the voltage ripple; however the decaps are effective on the eye-opening and jitter due to the impedance differences in the range 50MHz-700MHz (see Fig. 2b), where two impedance peaks at 65 MHz and 500 MHz occur.



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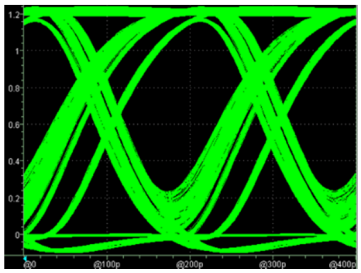
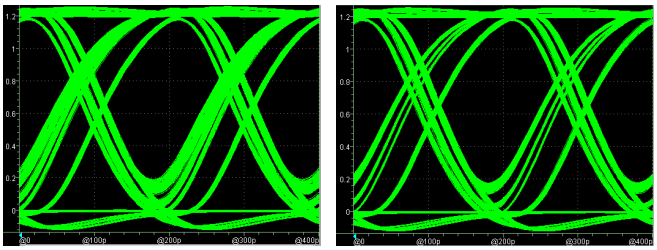


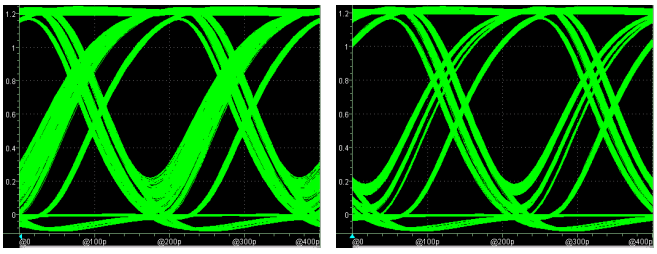
(c)

Fig. 6. The eye-diagram of the output of Port 3. (a) Case with no decaps. The voltage ripple at the power net of the I/O drive is 127mV. (b) Case with decaps at I/O ports with ESL = 0 pH. The voltage ripple is 107 mV. (c) Case with decaps at I/O ports with ESL = 50 pH. The voltage ripple is 112 mV.

During the interposer and chip PDN design, beside the decap inductance, the number and values of the decaps has influence on the I/O signal outputs. Fig. 7 shows the eye-diagram of the outputs when the decaps are placed on the grid as in Fig. 1, and directly at the I/O port (in both cases the ESL is 50pH). Both the voltage ripple and the eye-diagram jitter are the lowest at Port 1 where 4 decaps are added; the results at Port 3 are the worst due to the lack of decaps close to the port. Although the impedance profile in Fig. 3a are very similar, the small impact of the decaps on the input impedance within the whole frequency range considered still lead to significant improvement of the voltage ripple and jitter (eye diagram) when the decaps are placed close to the ports (Fig. 7a vs. Fig. 7b vs. Fig. 7c). The three comparisons in each sub-figure in Fig. 7 highlight the impact of the UC inductance in terms of PSIJ, that is summed up to the effect of the decap number, as mentioned above.



(a)



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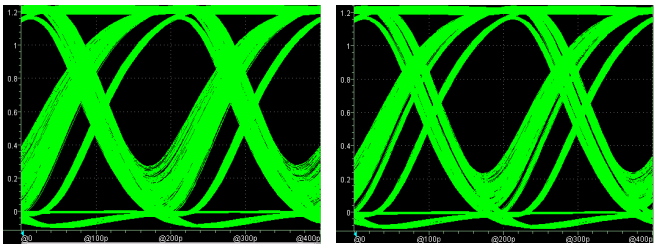

(c)

Fig. 7. The eye-diagram for the case of decaps at grid (ESL = 50 pH) on the left, and at I/O (ESL = 50 pH, on the right). (a) Output at Port 1, the voltage ripple is 100 mV (left) and 73.4 mV (right). (b) Output at Port 2, voltage ripple 104 mV (left) and 77.7 mV (right). (c) Output at Port 3, voltage ripple 117 mV (left) and 112 mV (right).

IV. Discussion and Conclusion

In general the larger the ESL is the higher is the voltage ripple generated and thus the noise and, consequently, the jitter, induced on the output signal. Thus the improvement of the chip/interposer PDN design could be achieved by an appropriate number and location of decaps associated to low ESL values. Even limited reduction of the PDN impedance leads to large impact on the time signals in terms of voltage ripple and eye diagrams. The target (best) design limit is set by the ideal case of no decap inductance. This case is useful to avoid any overdesign of PDN by placing unnecessary and expensive low-inductance decaps.

However, when an equivalent circuit model based on assembled UC array is used for the PDN, the designer should keep in mind the intrinsic value of the UC inductance; to this aim, whenever the decap is placed close to the I/O port with respect to the UC size, the I/O to decap inductance should be carefully evaluated and explicitly inserted on the decap equivalent model.

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